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Zhang et al.

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(54) **SYSTEMS AND METHODS FOR DATA PROCESSING USING GLOBAL ITERATION RESULT REUSE**

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H03M 13/11	(2006.01)
H03M 13/27	(2006.01)
H03M 13/00	(2006.01)
H03M 13/29	(2006.01)

(52) **U.S. Cl.**

CPC ***G06F 11/1076*** (2013.01); ***H03M 13/1111*** (2013.01); ***H03M 13/27*** (2013.01); ***H03M 13/2957*** (2013.01); ***H03M 13/6331*** (2013.01); ***H03M 13/658*** (2013.01); ***H03M 13/6583*** (2013.01); *H03M 13/2948* (2013.01); *H04L 2201/06* (2013.01)

(58) **Field of Classification Search**

CPC H04L 2201/06; H03M 13/2948; H03M 13/1102

USPC 714/774, 758

See application file for complete search history.

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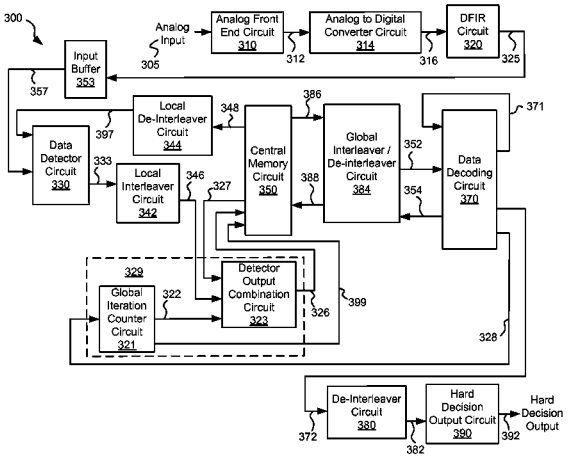
Primary Examiner — M. Mujtaba K Chaudry

(57) **ABSTRACT**

The present inventions are related to systems and methods for data processing, and more particularly to systems and methods for use of a detector output by a data decoder. As an example, a data processing system is discussed that includes a data detector circuit operable to provide a first detector output and a second detector output, and a combining circuit operable to combine a first input derived from the first detector output with a second input derived from the second detector output to yield a combined detector output. The combined detector output includes a unified data set element generated by combining an element of the first input with a corresponding element of the second input.

20 Claims, 6 Drawing Sheets



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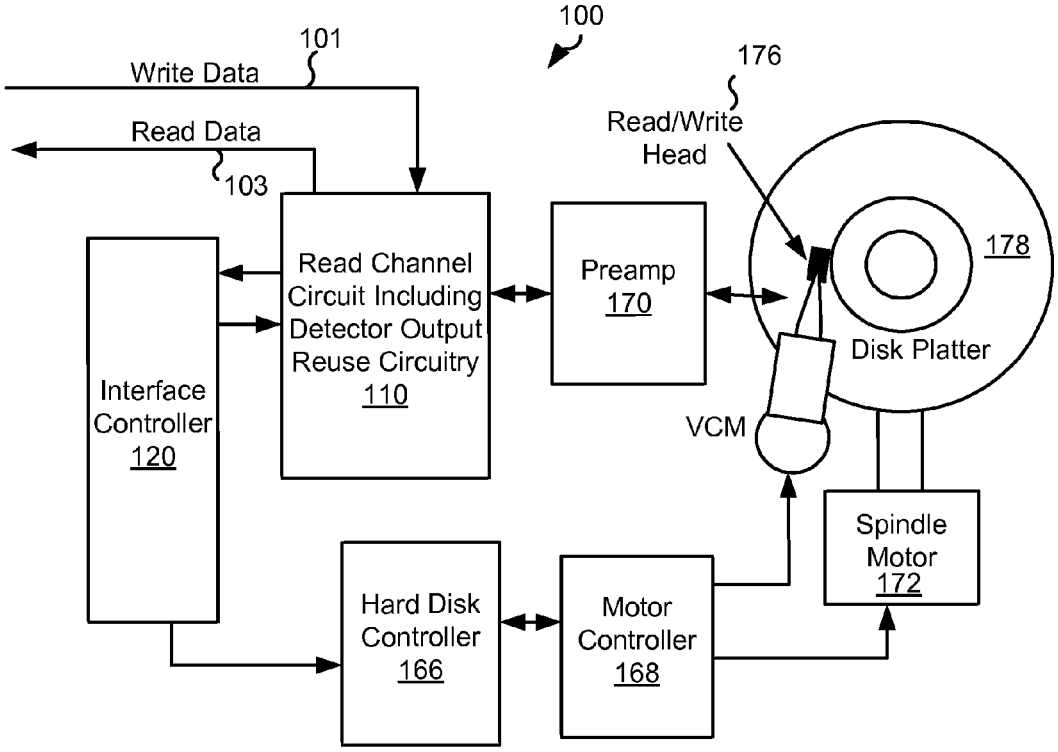
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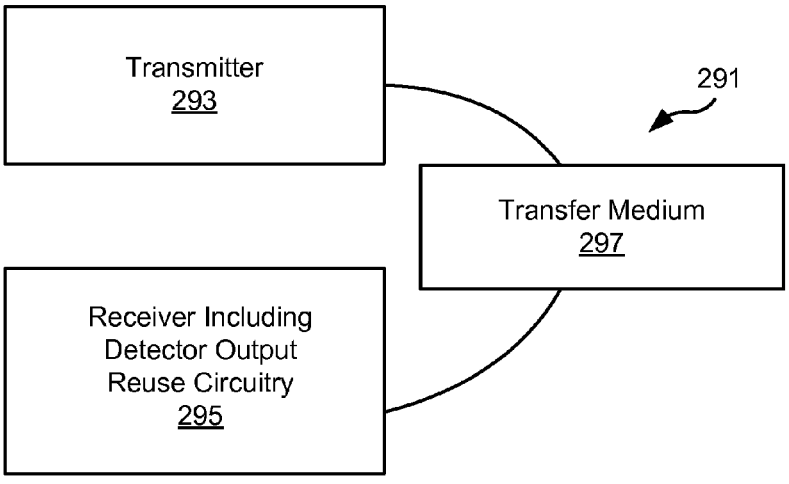
101
Write Data
Read Data
103
176
Read/Write Head
178
Disk Platter
VCM
Read Channel Circuit Including Detector Output Reuse Circuitry 110
Preamp 170
Interface Controller 120
Hard Disk Controller 166
Motor Controller 168
Spindle Motor 172

Fig. 1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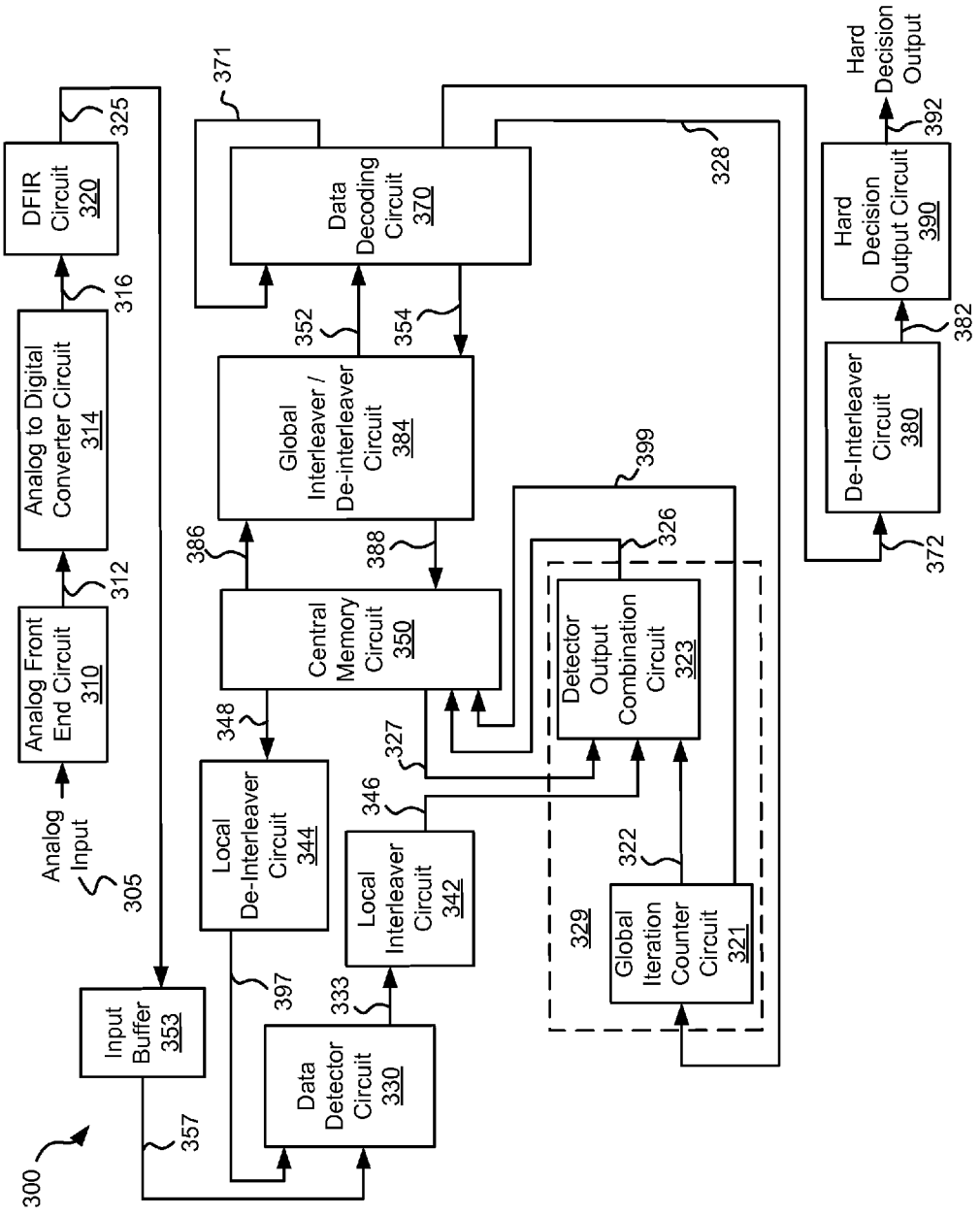
Transfer Medium 297
Receiver Including Detector Output Reuse Circuitry 295

Fig. 2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Analog Front End Circuit 310
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Analog to Digital Converter Circuit 314
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DFIR Circuit 320
325
Input Buffer 353
357
Data Detector Circuit 330
333
Local Interleaver Circuit 342
346
Local De-Interleaver Circuit 344
348
Central Memory Circuit 350
386
388
Global Interleaver / De-interleaver Circuit 384
352
354
Data Decoding Circuit 370
371
397
399
327
326
Detector Output Combination Circuit 323
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Global Iteration Counter Circuit 321
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372
De-Interleaver Circuit 380
382
Hard Decision Output Circuit 390
392
Hard Decision Output

Fig. 3

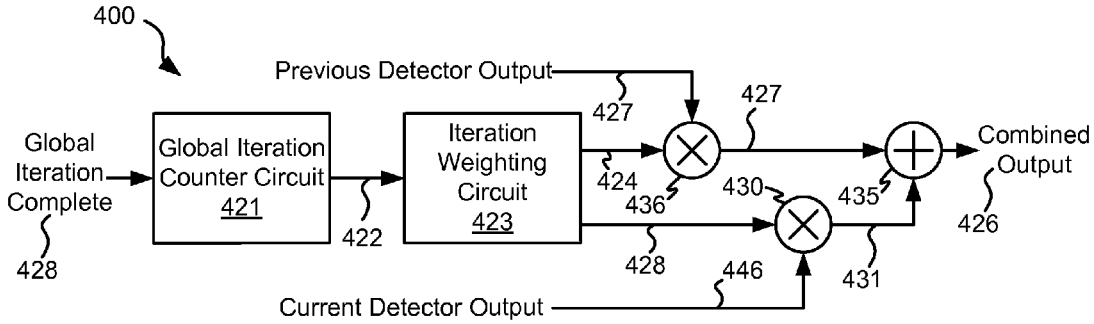

Fig. 4a

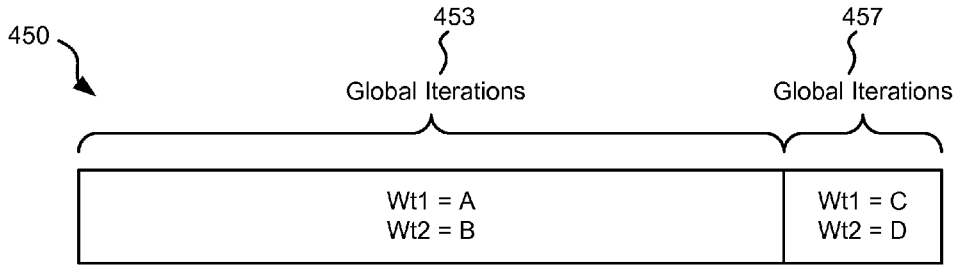

Fig. 4b

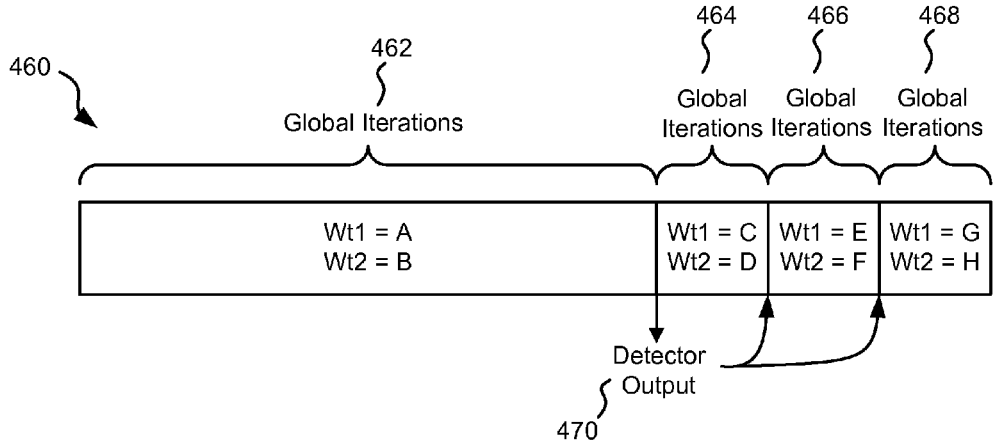

Fig. 4c

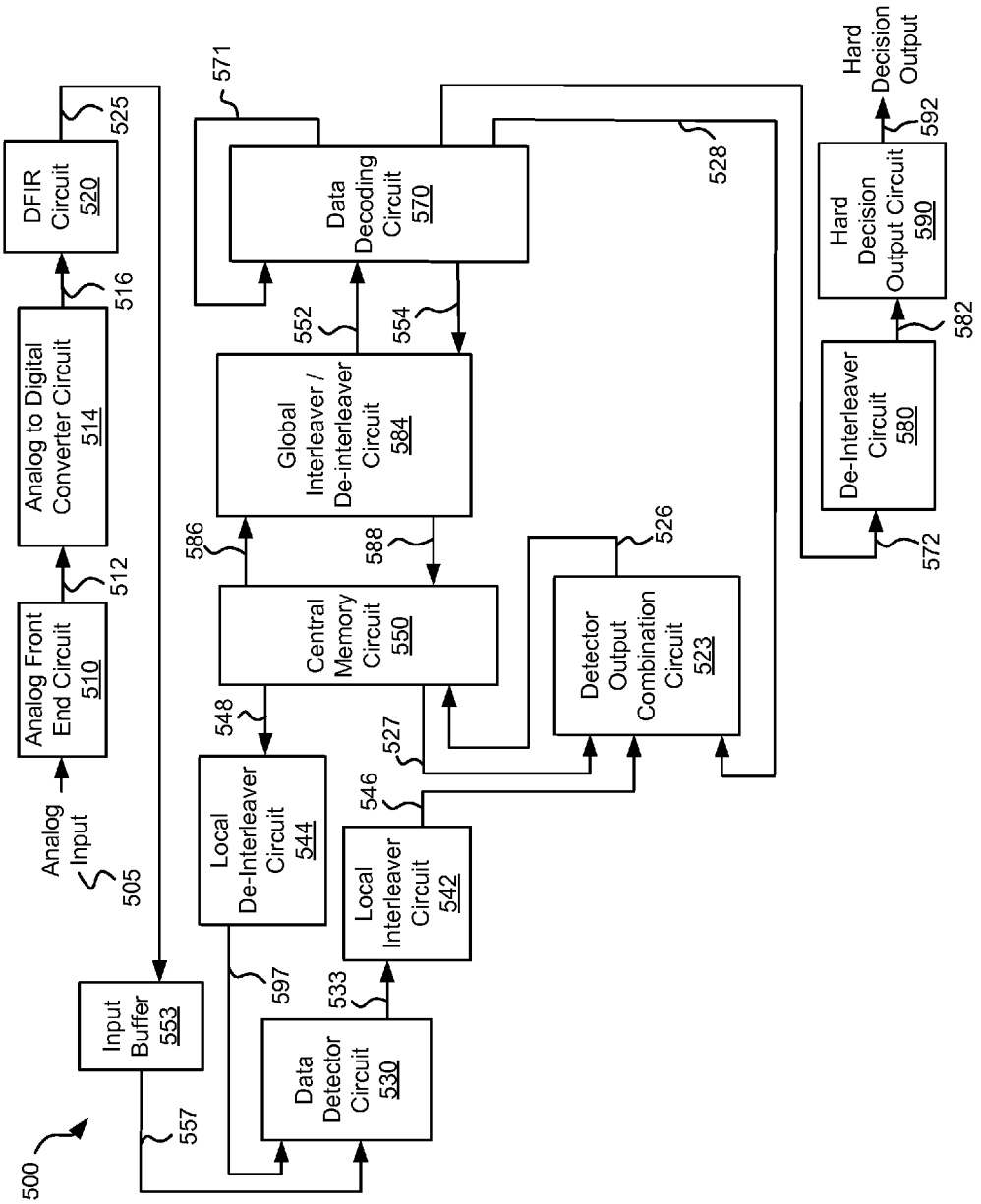
500
Analog Input
505
Analog Front End Circuit 510
512
Analog to Digital Converter Circuit 514
516
DFIR Circuit 520
525
Input Buffer 553
557
Data Detector Circuit 530
533
Local Interleaver Circuit 542
546
Local De-Interleaver Circuit 544
548
597
Central Memory Circuit 550
586
588
Global Interleaver / De-interleaver Circuit 584
552
554
571
Data Decoding Circuit 570
528
526
Detector Output Combination Circuit 523
527
572
De-Interleaver Circuit 580
582
Hard Decision Output Circuit 590
592
Hard Decision Output

Fig. 5

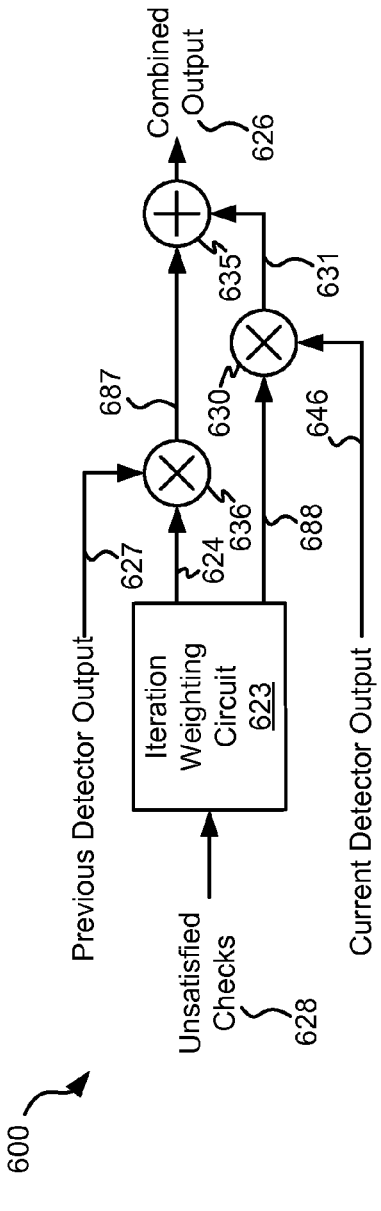
600
Previous Detector Output
627
Unsatisfied Checks
628
Iteration Weighting Circuit 623
624
636
688
687
630
646
635
631
Combined Output
626
Current Detector Output

Fig. 6

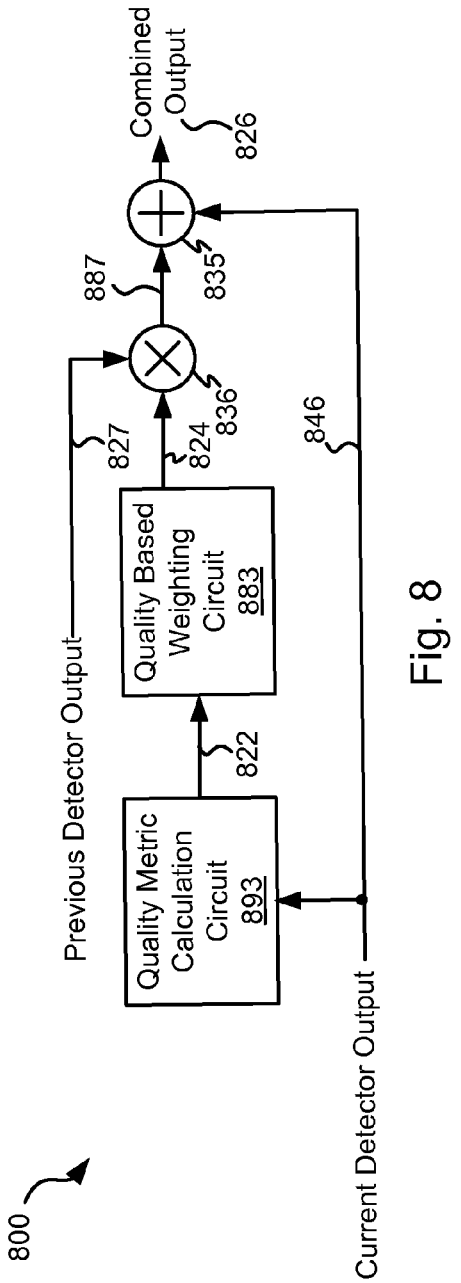
800
Previous Detector Output
827
Quality Metric Calculation Circuit 893
822
Quality Based Weighting Circuit 883
824
836
887
835
846
Combined Output
826
Current Detector Output

Fig. 8

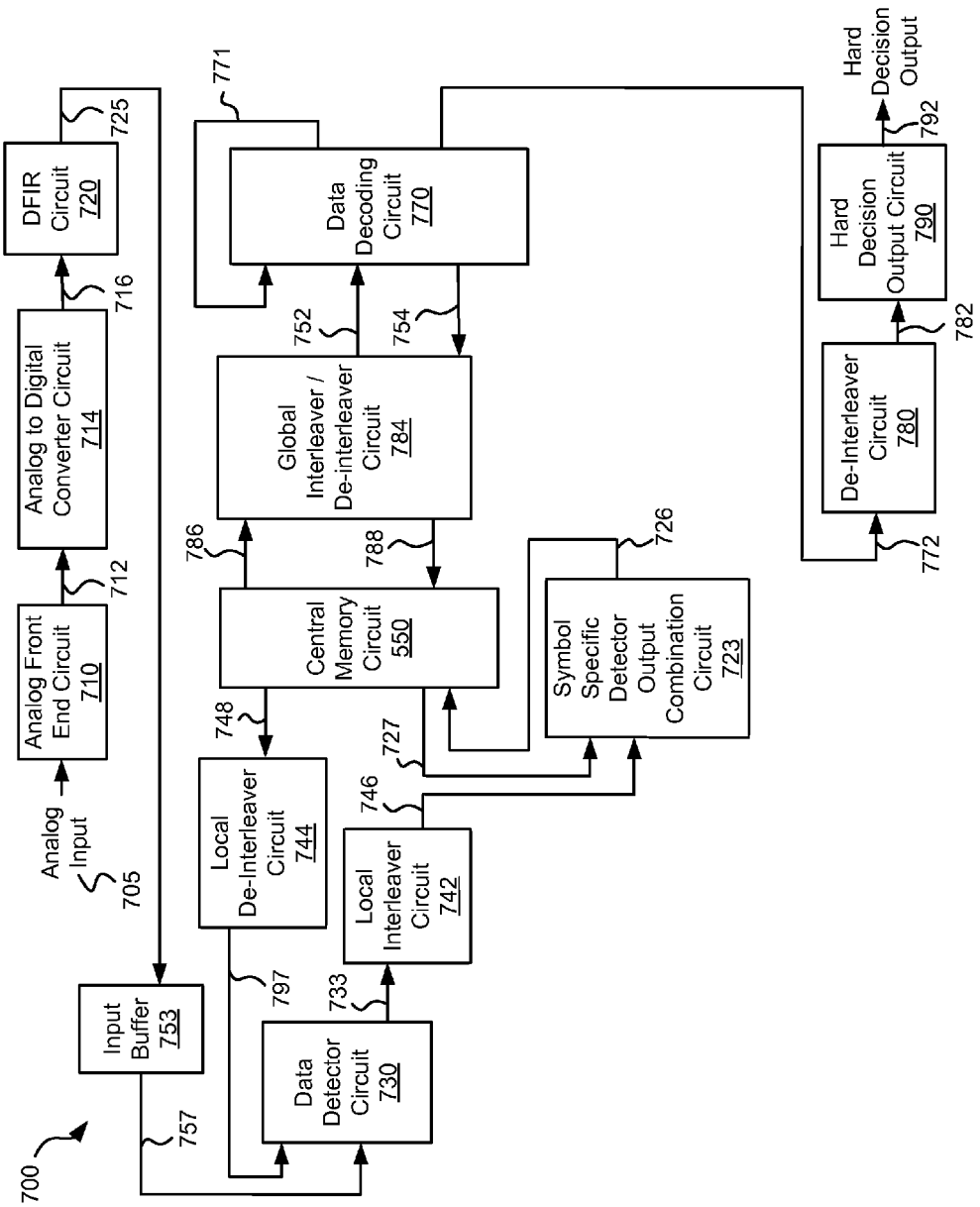
700
Input Buffer 753
757
Analog Input 705
Analog Front End Circuit 710
712
Analog to Digital Converter Circuit 714
716
DFIR Circuit 720
725
Data Detector Circuit 730
733
Local Interleaver Circuit 742
746
Local De-Interleaver Circuit 744
748
797
Central Memory Circuit 550
786
788
Global Interleaver / De-interleaver Circuit 784
752
754
771
Data Decoding Circuit 770
Symbol Specific Detector Output Combination Circuit 723
726
727
De-Interleaver Circuit 780
772
782
Hard Decision Output Circuit 790
792
Hard Decision Output

Fig. 7

SYSTEMS AND METHODS FOR DATA PROCESSING USING GLOBAL ITERATION RESULT REUSE

CROSS REFERENCE TO RELATED APPLICATIONS

The present application claims priority to (is a non-provisional of) U.S. Pat. App. No. 61/828,078, entitled "Systems and Methods for Data Processing Using Global Iteration Result Reuse", and filed May 28, 2013 by Zhang et al. The entirety of the aforementioned provisional patent application is incorporated herein by reference for all purposes.

BACKGROUND OF THE INVENTION

The present inventions are related to systems and methods for data processing, and more particularly to systems and methods for use of a detector output by a data decoder.

Various data transfer systems have been developed including storage systems, cellular telephone systems, radio transmission systems. In each of the systems data is transferred from a sender to a receiver via some medium. For example, in a storage system, data is sent from a sender (i.e., a write function) to a receiver (i.e., a read function) via a storage medium. In some cases, the data processing function uses a variable number of iterations through a data detector circuit and/or data decoder circuit depending upon the characteristics of the data being processed. Depending upon a number of factors, different data sets require more or fewer iterations through the data detector circuit and/or the data decoder circuit. In some cases, a data set being processed through a data processing circuit will not converge regardless of the number of iterations through the data detector circuit and/or the data decoder circuit.

Hence, for at least the aforementioned reasons, there exists a need in the art for advanced systems and methods for data processing.

BRIEF SUMMARY OF THE INVENTION

The present inventions are related to systems and methods for data processing, and more particularly to systems and methods for use of a detector output by a data decoder.

Some embodiments of the present invention provide data processing systems that include: a data detector circuit, a combining circuit, and a data decoder circuit. The data detector circuit is operable to apply a data detection algorithm to a data input to yield a first detector output, and to reapply the data detection algorithm to the data input to yield a second detector output. The combining circuit is operable to combine a first input derived from the first detector output with a second input derived from the second detector output to yield a combined detector output. The data decoder circuit is operable to apply a data decoding algorithm to a decoder input derived from the combined detector output to yield a decoded output.

This summary provides only a general outline of some embodiments of the invention. The phrases "in one embodiment," "according to one embodiment," "in various embodiments", "in one or more embodiments", "in particular embodiments" and the like generally mean the particular feature, structure, or characteristic following the phrase is included in at least one embodiment of the present invention, and may be included in more than one embodiment of the present invention. Importantly, such phases do not necessarily refer to the same embodiment. Many other embodiments of the invention will become more fully apparent from the following detailed description, the appended claims and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

A further understanding of the various embodiments of the present invention may be realized by reference to the figures which are described in remaining portions of the specification. In the figures, like reference numerals are used throughout several figures to refer to similar components. In some instances, a sub-label consisting of a lower case letter is associated with a reference numeral to denote one of multiple similar components. When reference is made to a reference numeral without specification to an existing sub-label, it is intended to refer to all such multiple similar components.

FIG. **1** shows a storage system including detector output reuse circuitry in accordance with various embodiments of the present invention;

FIG. **2** depicts a data transmission system including detector output reuse circuitry in accordance with one or more embodiments of the present invention;

FIG. **3** shows a data processing system including detector output reuse circuitry in accordance with some embodiments of the present invention;

FIG. **4***a* shows one implementation of a data detector output combination circuit that may be used in relation to the embodiments of FIG. **3**;

FIGS. **4***b*-**4***c* show different uses of the data detector output combination circuit of FIG. **4***a* that may be used in relation to various embodiments of the present invention;

FIG. **5** depicts another data processing system including detector output reuse circuitry in accordance with some embodiments of the present invention;

FIG. **6** shows an example implementation of a data detector output combination circuit that may be used in relation to the embodiments of FIG. **5**;

FIG. **7** depicts yet another data processing system including detector output reuse circuitry in accordance with some embodiments of the present invention; and

FIG. **8** shows an example implementation of a data detector output combination circuit that may be used in relation to the embodiments of FIG. **7**.

DETAILED DESCRIPTION OF THE INVENTION

The present inventions are related to systems and methods for data processing, and more particularly to systems and methods for use of a detector output by a data decoder.

Iterative data processing may include a data detector circuit that applies a data detection algorithm to a data set to yield a detected output, and a data decoder circuit that applies a data decoding algorithm to a decoder input derived from the detected output to yield a decoded output. The process of passing data through both the data detector circuit and the data decoder circuit is referred to herein as a "global iteration". During each global iteration, the data decoding algorithm may be repeatedly applied to a processing data set. This reapplication of the data decoding algorithm is referred to herein as a "local iteration". In particular embodiments of the present invention, a default number of ten local iterations are allowed for each global iteration. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of numbers of local iterations that may be used as a default in relation to different embodiments of the present invention. In some circuits where out of order result reporting

is allowed, a large number of global iterations (e.g., 120) for a given data set may be supported.

Some embodiments of the present invention provide data processing systems that include: a data detector circuit, a combining circuit, and a data decoder circuit. The data detector circuit is operable to apply a data detection algorithm to a data input to yield a first detector output, and to reapply the data detection algorithm to the data input to yield a second detector output. The combining circuit is operable to combine a first input derived from the first detector output with a second input derived from the second detector output to yield a combined detector output. The data decoder circuit is operable to apply a data decoding algorithm to a decoder input derived from the combined detector output to yield a decoded output. In some instances of the aforementioned embodiments, the decoder input is a first instance of the decoder input, and in reapplying the data detection algorithm to the data input to yield the second detector output is guided by a second instance of the decoder input. In some cases, the system is implemented as an integrated circuit. In various cases, the system is implemented as part of a communication device, and in other cases, the system is implemented as part of a storage device. In one or more cases, the data decoder circuit is a low density parity check decoder circuit. In some cases, the data detection algorithm is a Viterbi data detection algorithm. In other cases, the data detection algorithm is a maximum a posterior data detection algorithm.

In some instances of the aforementioned embodiments, applying the data detection algorithm and applying the data decoding algorithm at least one time corresponds to a global iteration. In such instances, the combining the first input and the second input is done in a proportion based upon a number of global iterations. In some cases, the first input and the second input are combined in a first proportion when a number of global iterations is less than a threshold value. In such cases, the first input and the second input are combined in a second proportion when the number of global iterations is greater than the threshold value. In various cases, the combined detector output is a first combined detector output, and the threshold value is a first threshold value. In such cases, the data detector circuit may be further operable to apply the data detection algorithm to the data input to yield a third detector output where the third detector output occurs coincident to the first threshold value. The combining circuit is further operable to combine the second input with a third input derived from the third detector output to yield a second combined detector output when the number of global iterations is equal to a second threshold value.

In other instances of the aforementioned embodiments, the data decoder circuit is further operable to provide a number of unsatisfied checks remaining in the decoded output, and the combining circuit is operable to combine the first input with the second input in a proportion based upon the number of unsatisfied checks. In yet other instances of the aforementioned embodiments, the combining circuit is further operable to generate a quality metric indicative of a quality of an element of the first input, and the combining circuit is operable to combine the first input with the second input in a proportion based upon the quality metric.

Other embodiments of the present invention provide methods for data processing that include: applying a data detection algorithm using a data detector circuit to a data input to yield a first detector output; re-applying the data detection algorithm using the data detector circuit to the data input to yield a second detector output; combining a first input derived from the first detector output with a second input derived from the second detector output to yield a combined detector output; and applying a data decoding algorithm using a data decoder circuit to a decoder input derived from the combined detector output to yield a decoded output. In some instances of the aforementioned embodiments, applying the data detection algorithm and applying the data decoding algorithm at least one time corresponds to a global iteration, and the first input and the second input in a proportion based upon a number of global iterations. In some cases, the first input and the second output are combined in a first proportion when a number of global iterations is less than a threshold value, and the first input and the second input are combined in a second proportion when the number of global iterations is greater than the threshold value. In some particular cases, the combined detector output is a first combined detector output, and the threshold value is a first threshold value. In such cases, the methods further include: re-applying the data detection algorithm to the data input to yield a third detector output where the third detector output occurs coincident to the first threshold value. The combining the second input with a third input derived from the third detector output to yield a second combined detector output when the number of global iterations is equal to a second threshold value.

In other instances of the aforementioned embodiments, the methods further include: generating a number of unsatisfied checks remaining in the decoded output, and the combining the first input with the second input is done in a proportion based upon the number of unsatisfied checks. In yet other instances of the aforementioned embodiments, the methods further include: generating a quality metric indicative of a quality of an element of the first input, and the combining the first input with the second input is done in a proportion based upon the quality metric.

Turning to FIG. **1**, a storage system **100** including a read channel circuit **110** having detector output reuse circuitry is shown in accordance with various embodiments of the present invention. Storage system **100** may be, for example, a hard disk drive. Storage system **100** also includes a preamplifier **170**, an interface controller **120**, a hard disk controller **166**, a motor controller **168**, a spindle motor **172**, a disk platter **178**, and a read/write head **176**. Interface controller **120** controls addressing and timing of data to/from disk platter **178**. The data on disk platter **178** consists of groups of magnetic signals that may be detected by read/write head assembly **176** when the assembly is properly positioned over disk platter **178**. In one embodiment, disk platter **178** includes magnetic signals recorded in accordance with either a longitudinal or a perpendicular recording scheme.

In operation, read/write head assembly **176** is accurately positioned by motor controller **168** over a desired data track on disk platter **178**. Motor controller **168** both positions read/write head assembly **176** in relation to disk platter **178** and drives spindle motor **172** by moving read/write head assembly to the proper data track on disk platter **178** under the direction of hard disk controller **166**. Spindle motor **172** spins disk platter **178** at a determined spin rate (RPMs). Once read/write head assembly **176** is positioned adjacent the proper data track, magnetic signals representing data on disk platter **178** are sensed by read/write head assembly **176** as disk platter **178** is rotated by spindle motor **172**. The sensed magnetic signals are provided as a continuous, minute analog signal representative of the magnetic data on disk platter **178**. This minute analog signal is transferred from read/write head assembly **176** to read channel circuit **110** via preamplifier **170**. Preamplifier **170** is operable to amplify the minute analog signals accessed from disk platter **178**. In turn, read channel circuit **110** decodes and digitizes the received analog signal to recreate the information originally written to disk

platter **178**. This data is provided as read data **103**. The opposite is a write operation where write data **101** is provided to read channel circuit **110** that encodes the data and stores it to disk platter **178** via preamplifier **170** and read/write head assembly **176**.

As part of processing data accessed from disk platter **178**, read channel circuit **110** applies a data detection algorithm to data accessed from disk platter **178** to yield a detected output. Under some conditions, a prior detected output may be combined with the current detected output to yield a combined detected output. A data decoder circuit applies a data decode algorithm to the combined detected output to yield a decoder output. Where the decoder output does not exhibit any remaining errors, it is provided as read data **103**. In some cases, read channel circuit **110** may include a data processing circuit similar to that discussed below in relation to FIG. **3** or FIG. **5** below, and may operate similar to that discussed below in relation to FIGS. **7***a*-**7***c* below.

It should be noted that storage system **100** may be integrated into a larger storage system such as, for example, a RAID (redundant array of inexpensive disks or redundant array of independent disks) based storage system. Such a RAID storage system increases stability and reliability through redundancy, combining multiple disks as a logical unit. Data may be spread across a number of disks included in the RAID storage system according to a variety of algorithms and accessed by an operating system as if it were a single disk. For example, data may be mirrored to multiple disks in the RAID storage system, or may be sliced and distributed across multiple disks in a number of techniques. If a small number of disks in the RAID storage system fail or become unavailable, error correction techniques may be used to recreate the missing data based on the remaining portions of the data from the other disks in the RAID storage system. The disks in the RAID storage system may be, but are not limited to, individual storage systems such as storage system **100**, and may be located in close proximity to each other or distributed more widely for increased security. In a write operation, write data is provided to a controller, which stores the write data across the disks, for example by mirroring or by striping the write data. In a read operation, the controller retrieves the data from the disks. The controller then yields the resulting read data as if the RAID storage system were a single disk.

A data decoder circuit used in relation to read channel circuit **110** may be, but is not limited to, a low density parity check (LDPC) decoder circuit as are known in the art. Such low density parity check technology is applicable to transmission of information over virtually any channel or storage of information on virtually any media. Transmission applications include, but are not limited to, optical fiber, radio frequency channels, wired or wireless local area networks, digital subscriber line technologies, wireless cellular, Ethernet over any medium such as copper or optical fiber, cable channels such as cable television, and Earth-satellite communications. Storage applications include, but are not limited to, hard disk drives, compact disks, digital video disks, magnetic tapes and memory devices such as DRAM, NAND flash, NOR flash, other non-volatile memories and solid state drives.

In addition, it should be noted that storage system **100** may be modified to include solid state memory that is used to store data in addition to the storage offered by disk platter **178**. This solid state memory may be used in parallel to disk platter **178** to provide additional storage. In such a case, the solid state memory receives and provides information directly to read channel circuit **110**. Alternatively, the solid state memory may be used as a cache where it offers faster access time than that offered by disk platted **178**. In such a case, the solid state memory may be disposed between interface controller **120** and read channel circuit **110** where it operates as a pass through to disk platter **178** when requested data is not available in the solid state memory or when the solid state memory does not have sufficient storage to hold a newly written data set. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of storage systems including both disk platter **178** and a solid state memory.

Turning to FIG. **2**, a data transmission system **291** including a receiver **295** having floating variance calibration and detection circuitry is shown in accordance with various embodiments of the present invention. Data transmission system **291** includes a transmitter **293** that is operable to transmit encoded information via a transfer medium **297** as is known in the art. The encoded information is received from transfer medium **297** by a receiver **295**. Receiver **295** processes a received input representing the encoded information to yield the originally transmitted data.

As part of processing data received by receiver **295**, receiver **295** applies a data detection algorithm to data received from transfer medium **297** to yield a detected output. Under some conditions, a prior detected output may be combined with the current detected output to yield a combined detected output. A data decoder circuit applies a data decode algorithm to the combined detected output to yield a decoder output. Where the decoder output does not exhibit any remaining errors, it is provided as a data output. In some cases, receiver **295** may include a data processing circuit similar to that discussed below in relation to FIG. **3** or FIG. **5** below, and may operate similar to that discussed below in relation to FIGS. **7***a*-**7***c* below.

Turning to FIG. **3**, a data processing system **300** including detector output reuse circuitry is shown in accordance with some embodiments of the present invention. Data processing system **300** includes an analog front end circuit **310** that receives an analog signal **305**. Analog front end circuit **310** processes analog signal **305** and provides a processed analog signal **312** to an analog to digital converter circuit **314**. Analog front end circuit **310** may include, but is not limited to, an analog filter and an amplifier circuit as are known in the art. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of circuitry that may be included as part of analog front end circuit **310**. In some cases, analog signal **305** is derived from a read/write head assembly (not shown) that is disposed in relation to a storage medium (not shown). In other cases, analog signal **305** is derived from a receiver circuit (not shown) that is operable to receive a signal from a transmission medium (not shown). The transmission medium may be wired or wireless. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of source from which analog input **305** may be derived.

Analog to digital converter circuit **314** converts processed analog signal **312** into a corresponding series of digital samples **316**. Analog to digital converter circuit **314** may be any circuit known in the art that is capable of producing digital samples corresponding to an analog input signal. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of analog to digital converter circuits that may be used in relation to different embodiments of the present invention. Digital samples **316** are provided to an equalizer circuit **320**. Equalizer circuit **320** applies an equalization algorithm to digital samples **316** to yield an equalized output **325**. In some embodiments of the present invention, equalizer circuit **320** is a digital finite impulse response filter circuit as are known in the art. It may

be possible that equalized output **325** may be received directly from a storage device in, for example, a solid state storage system. In such cases, analog front end circuit **310**, analog to digital converter circuit **314** and equalizer circuit **320** may be eliminated where the data is received as a digital data input. Equalized output **325** is stored to an input buffer **353** that includes sufficient memory to maintain one or more codewords until processing of that codeword is completed through a data detector circuit **330** and a data decoding circuit **370** including, where warranted, multiple global iterations (passes through both data detector circuit **330** and data decoding circuit **370**) and/or local iterations (passes through data decoding circuit **370** during a given global iteration). An output **357** is provided to data detector circuit **330**.

Data detector circuit **330** may be a single data detector circuit or may be two or more data detector circuits operating in parallel on different codewords. Whether it is a single data detector circuit or a number of data detector circuits operating in parallel, data detector circuit **330** is operable to apply a data detection algorithm to a received codeword or data set. In some embodiments of the present invention, data detector circuit **330** is a Viterbi algorithm data detector circuit as are known in the art. In other embodiments of the present invention, data detector circuit **330** is a is a maximum a posteriori data detector circuit as are known in the art. Of note, the general phrases "Viterbi data detection algorithm" or "Viterbi algorithm data detector circuit" are used in their broadest sense to mean any Viterbi detection algorithm or Viterbi algorithm detector circuit or variations thereof including, but not limited to, bi-direction Viterbi detection algorithm or bi-direction Viterbi algorithm detector circuit. Also, the general phrases "maximum a posteriori data detection algorithm" or "maximum a posteriori data detector circuit" are used in their broadest sense to mean any maximum a posteriori detection algorithm or detector circuit or variations thereof including, but not limited to, simplified maximum a posteriori data detection algorithm and a max-log maximum a posteriori data detection algorithm, or corresponding detector circuits. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of data detector circuits that may be used in relation to different embodiments of the present invention. In some cases, one data detector circuit included in data detector circuit **330** is used to apply the data detection algorithm to the received codeword for a first global iteration applied to the received codeword, and another data detector circuit included in data detector circuit **330** is operable apply the data detection algorithm to the received codeword guided by a decoded output accessed from a central memory circuit **350** on subsequent global iterations.

Upon completion of application of the data detection algorithm to the received codeword on the first global iteration, data detector circuit **330** provides a detector output **333**. Detector output **333** includes soft data. As used herein, the phrase "soft data" is used in its broadest sense to mean reliability data with each instance of the reliability data indicating a likelihood that a corresponding bit position or group of bit positions has been correctly detected. In some embodiments of the present invention, the soft data or reliability data is log likelihood ratio data as is known in the art. Detector output **333** is provided to a local interleaver circuit **342**. Local interleaver circuit **342** is operable to shuffle sub-portions (i.e., local chunks) of the data set included as detected output and provides an interleaved codeword **346**. Interleaver circuit **342** may be any circuit known in the art that is capable of shuffling data sets to yield a re-arranged data set.

Interleaved codeword **346** is provided to an output combination circuit **329** where it is combined with a previous interleaved codeword **327** accessed from central memory circuit **350** to yield a combined output **326**. Previous interleaved codeword **327** is derived from a detector output **333** resulting from a previous global iteration. Combined output **326** is stored to central memory circuit **350** as the current interleaved output, and the previous interleaved output is updated to be the current interleaved output in preparation for the next global iteration. The operation of output combination circuit **329** is discussed below in more detail.

Once a data decoding circuit **370** is available, the current interleaved output (i.e., the current instance of combined codeword **326**) is accessed from central memory circuit **350** as a stored codeword **386** and globally interleaved by a global interleaver/de-interleaver circuit **384**. Global interleaver/De-interleaver circuit **384** may be any circuit known in the art that is capable of globally rearranging codewords. Global interleaver/De-interleaver circuit **384** provides a decoder input **352** into data decoding circuit **370**. In some embodiments of the present invention, the data decode algorithm is a low density parity check algorithm as are known in the art. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize other decode algorithms that may be used in relation to different embodiments of the present invention. Data decoding circuit **370** applies a data decode algorithm to decoder input **352** to yield a decoded output **371**. In cases where another local iteration (i.e., another pass through data decoder circuit **370**) is desired, data decoding circuit **370** re-applies the data decode algorithm to decoder input **352** guided by decoded output **371**. This continues until either a maximum number of local iterations is exceeded or decoded output **371** converges.

Where decoded output **371** fails to converge (i.e., fails to yield the originally written data set) and a number of local iterations through data decoder circuit **370** exceeds maximum number of allowable local iterations, the resulting decoded output is provided as a decoded output **354** back to central memory circuit **350** where it is stored awaiting another global iteration through a data detector circuit included in data detector circuit **330**. Prior to storage of decoded output **354** to central memory circuit **350**, decoded output **354** is globally de-interleaved to yield a globally de-interleaved output **388** that is stored to central memory circuit **350**. The global de-interleaving reverses the global interleaving earlier applied to stored codeword **386** to yield decoder input **352**. When a data detector circuit included in data detector circuit **330** becomes available, a previously stored de-interleaved output **388** accessed from central memory circuit **350** and locally de-interleaved by a de-interleaver circuit **344**. De-interleaver circuit **344** re-arranges decoder output **348** to reverse the shuffling originally performed by interleaver circuit **342**. A resulting de-interleaved output **397** is provided to data detector circuit **330** where it is used to guide subsequent detection of a corresponding data set previously received as equalized output **325**.

Alternatively, where the decoded output converges (i.e., yields the originally written data set), the resulting decoded output is provided as an output codeword **372** to a de-interleaver circuit **380**. De-interleaver circuit **380** rearranges the data to reverse both the global and local interleaving applied to the data to yield a de-interleaved output **382**. De-interleaved output **382** is provided to a hard decision output circuit **390**. Hard decision output circuit **390** is operable to re-order data sets that may complete out of order back into their original order. The originally ordered data sets are then provided as a hard decision output **392**.

Data decoding circuit **370** provides an end of global iteration output **328** to output combination circuit **329**. End of

global iteration output **328** is asserted high when the last local iteration is applied by data decoding circuit **370** to a given data set. Output combination circuit **329** includes a global iteration counter circuit **321** that is incremented each time end of global iteration output **328** is asserted to yield a global iteration count **322**. Of note, data processing system **300** is operable to process multiple data sets (i.e., sets of equalized data stored in input buffer **353**) concurrently. Thus, global iteration counter circuit **321** maintains a count of the number of global iterations for each of the data sets maintained in input buffer **353**. In addition, output combination circuit **329** includes a detector output combination circuit **323** that generates combined output **326** as a combination of interleaved codeword **346** and previous interleaved codeword **327** based upon global iteration count **322** for the currently processing data set. As an example, for a first number of global iterations, detector output combination circuit **323** may set combined output **326** equal to interleaved codeword **346**. For a subsequent number of global iterations, detector output combination circuit **323** may calculate combined output **326** as a weighted average of interleaved codeword **346** and previous interleaved codeword **327**.

Turning to FIG. **4***a*, one implementation of a data detector output combination circuit **400** is shown in accordance with some embodiments of the present invention. In some cases, data detector output combination circuit **400** may be used in place of output combination circuit **329**. In such cases, a global iteration complete signal **428** is connected to global iteration output **328**, a previous detector output **427** is connected to previous interleaved output **327**, a current detector output **446** is connected to interleaved output **346**, and a combined output **426** is connected to combined output **326**.

Data detector output combination circuit **400** includes a global iteration counter circuit **421** that is incremented each time global iteration complete signal **428** is asserted to yield a global iteration count **422**. Global iteration count **422** is provided to a iteration weighting circuit **423** that provides a previous data scalar value (Wt1) **424** and a current data scalar value (Wt2) **428**. Previous detector output **427** is multiplied by previous data scalar value **424** by a multiplier circuit **436** to yield a previous product **427**; and current detector output **446** is multiplied by current data scalar value **428** by a multiplier circuit **430** to yield a current product **431**. A summation circuit adds current product **431** to previous product **427** to yield combined output **426**. As shown in a timing diagram **450** of FIG. **4***b*, the values of Wt1 and Wt2 change after application of a defined number of global iterations **453**, with the new values being applied for a subsequent number of global iterations **457**. In particular, where the number of global iterations is less than global iterations **453**, the scalar values are, respectively:

Wt1=A and

Wt2=B.

In one particular embodiment of the present invention, the value of A is zero (0), and the value of B is one (1). Where the number of global iterations is greater than or equal to global iterations **453**, the scalar values are, respectively:

Wt1=C; and

Wt2=D.

In one particular embodiment of the present invention, the value of C is one (1), and the value of D is three (3). Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of different values for A, B, C and D that may be used in relation to different embodiments of the present invention. In one particular embodiment of the present invention, the number of global iterations **453** is one hundred ten (110). Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of different values for the number of global iterations **453** that may be used in relation to different embodiments of the present invention. Such values may be either fixed or programmable.

As shown in a timing diagram **460** of FIG. **4***c*, the values of Wt1 and Wt2 change after application of a defined number of global iterations **462**, with the new values being applied for a subsequent number of global iterations **464**. In particular, where the number of global iterations is less than global iterations **462**, the scalar values are, respectively:

Wt1=A; and

Wt2=B.

In one particular embodiment of the present invention, the value of A is zero (0), and the value of B is one (1). Where the number of global iterations is greater than or equal to global iterations **464**, and less than global iterations **462** plus global iterations **464**, the scalar values are, respectively:

Wt1=C; and

Wt2=D.

In one particular embodiment of the present invention, the value of C is one (1), and the value of D is three (3). During global iterations **464**, the initial processing is applied to a detector output **470** (i.e., the detector output at the end of global iterations **462**).

Where the decoding fails to converge after global iterations **462** plus global iterations **464**, the scalar values are changed to:

Wt1=E; and

Wt2=F.

In one particular embodiment of the present invention, the value of E is one (1), and the value of D is two (2). During global iterations **466**, the initial processing is applied to a detector output **470** (i.e., the detector output at the end of global iterations **462**), and the detector output at the end of global iterations **464** is discarded. Where the decoding fails to converge after global iterations **462** plus global iterations **464** and global iterations **466**, the scalar values are again changed to:

Wt1=G; and

Wt2=H.

In one particular embodiment of the present invention, the value of E is one (1), and the value of D is four (4). During global iterations **468**, the initial processing is applied to a detector output **470** (i.e., the detector output at the end of global iterations **462**), and the detector output at the end of global iterations **466** is discarded. Such an approach of changing scaling factors and reverting back to an earlier detector output allows for the use of multiple different pairs of scaling factors with propagating any results of a failed set of scaling factors. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of different values for A, B, C, D, E, F, G and H that may be used in relation to different embodiments of the present invention. Such values may be either fixed or programmable. In one particular embodiment of the present invention, the number of global iterations **453** is ninety (90), and each of the number of global iterations **464**, **466**, **468** are ten (10). Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of different values for the respective numbers of global iterations that may be used in relation to different embodiments of the present invention. Such values may be either fixed or programmable.

Turning to FIG. **5**, another data processing system **500** including detector output reuse circuitry is shown in accordance with some embodiments of the present invention. Data processing system **500** includes an analog front end circuit

510 that receives an analog signal 505. Analog front end circuit 510 processes analog signal 505 and provides a processed analog signal 512 to an analog to digital converter circuit 514. Analog front end circuit 510 may include, but is not limited to, an analog filter and an amplifier circuit as are known in the art. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of circuitry that may be included as part of analog front end circuit 510. In some cases, analog signal 505 is derived from a read/write head assembly (not shown) that is disposed in relation to a storage medium (not shown). In other cases, analog signal 505 is derived from a receiver circuit (not shown) that is operable to receive a signal from a transmission medium (not shown). The transmission medium may be wired or wireless. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of source from which analog input 505 may be derived.

Analog to digital converter circuit 514 converts processed analog signal 512 into a corresponding series of digital samples 516. Analog to digital converter circuit 514 may be any circuit known in the art that is capable of producing digital samples corresponding to an analog input signal. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of analog to digital converter circuits that may be used in relation to different embodiments of the present invention. Digital samples 516 are provided to an equalizer circuit 520. Equalizer circuit 520 applies an equalization algorithm to digital samples 516 to yield an equalized output 525. In some embodiments of the present invention, equalizer circuit 520 is a digital finite impulse response filter circuit as are known in the art. It may be possible that equalized output 525 may be received directly from a storage device in, for example, a solid state storage system. In such cases, analog front end circuit 510, analog to digital converter circuit 514 and equalizer circuit 520 may be eliminated where the data is received as a digital data input. Equalized output 525 is stored to an input buffer 553 that includes sufficient memory to maintain one or more codewords until processing of that codeword is completed through a data detector circuit 530 and a data decoding circuit 570 including, where warranted, multiple global iterations (passes through both data detector circuit 530 and data decoding circuit 570) and/or local iterations (passes through data decoding circuit 570 during a given global iteration). An output 557 is provided to data detector circuit 530.

Data detector circuit 530 may be a single data detector circuit or may be two or more data detector circuits operating in parallel on different codewords. Whether it is a single data detector circuit or a number of data detector circuits operating in parallel, data detector circuit 530 is operable to apply a data detection algorithm to a received codeword or data set. In some embodiments of the present invention, data detector circuit 530 is a Viterbi algorithm data detector circuit as are known in the art. In other embodiments of the present invention, data detector circuit 530 is a is a maximum a posteriori data detector circuit as are known in the art. Of note, the general phrases "Viterbi data detection algorithm" or "Viterbi algorithm data detector circuit" are used in their broadest sense to mean any Viterbi detection algorithm or Viterbi algorithm detector circuit or variations thereof including, but not limited to, bi-direction Viterbi detection algorithm or bi-direction Viterbi algorithm detector circuit. Also, the general phrases "maximum a posteriori data detection algorithm" or "maximum a posteriori data detector circuit" are used in their broadest sense to mean any maximum a posteriori detection algorithm or detector circuit or variations thereof including, but not limited to, simplified maximum a posteriori data detection algorithm and a max-log maximum a posteriori data detection algorithm, or corresponding detector circuits. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of data detector circuits that may be used in relation to different embodiments of the present invention. In some cases, one data detector circuit included in data detector circuit 530 is used to apply the data detection algorithm to the received codeword for a first global iteration applied to the received codeword, and another data detector circuit included in data detector circuit 530 is operable apply the data detection algorithm to the received codeword guided by a decoded output accessed from a central memory circuit 550 on subsequent global iterations.

Upon completion of application of the data detection algorithm to the received codeword on the first global iteration, data detector circuit 530 provides a detector output 533. Detector output 533 includes soft data. As used herein, the phrase "soft data" is used in its broadest sense to mean reliability data with each instance of the reliability data indicating a likelihood that a corresponding bit position or group of bit positions has been correctly detected. In some embodiments of the present invention, the soft data or reliability data is log likelihood ratio data as is known in the art. Detector output 533 is provided to a local interleaver circuit 542. Local interleaver circuit 542 is operable to shuffle sub-portions (i.e., local chunks) of the data set included as detected output and provides an interleaved codeword 546. Interleaver circuit 542 may be any circuit known in the art that is capable of shuffling data sets to yield a re-arranged data set.

Interleaved codeword 546 is provided to a detector output combination circuit 523 where it is combined with a previous interleaved codeword 527 accessed from central memory circuit 550 to yield a combined output 526. Previous interleaved codeword 527 is derived from a detector output 533 resulting from a previous global iteration. Combined output 526 is stored to central memory circuit 550 as the current interleaved output, and the previous interleaved output is updated to be the current interleaved output in preparation for the next global iteration. The operation of detector output combination circuit 523 is discussed below in more detail.

Once a data decoding circuit 570 is available, the current interleaved output (i.e., the current instance of combined codeword 526) is accessed from central memory circuit 550 as a stored codeword 586 and globally interleaved by a global interleaver/de-interleaver circuit 584. Global interleaver/De-interleaver circuit 584 may be any circuit known in the art that is capable of globally rearranging codewords. Global interleaver/De-interleaver circuit 584 provides a decoder input 552 into data decoding circuit 570. In some embodiments of the present invention, the data decode algorithm is a low density parity check algorithm as are known in the art. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize other decode algorithms that may be used in relation to different embodiments of the present invention. Data decoding circuit 570 applies a data decode algorithm to decoder input 552 to yield a decoded output 571. In cases where another local iteration (i.e., another pass through data decoder circuit 570) is desired, data decoding circuit 570 re-applies the data decode algorithm to decoder input 552 guided by decoded output 571. This continues until either a maximum number of local iterations is exceeded or decoded output 571 converges.

Where decoded output 571 fails to converge (i.e., fails to yield the originally written data set) and a number of local iterations through data decoder circuit 570 exceeds maximum number of allowable local iterations, the resulting decoded output is provided as a decoded output 554 back to central

memory circuit **550** where it is stored awaiting another global iteration through a data detector circuit included in data detector circuit **530**. Prior to storage of decoded output **554** to central memory circuit **550**, decoded output **554** is globally de-interleaved to yield a globally de-interleaved output **588** that is stored to central memory circuit **550**. The global de-interleaving reverses the global interleaving earlier applied to stored codeword **586** to yield decoder input **552**. When a data detector circuit included in data detector circuit **530** becomes available, a previously stored de-interleaved output **588** accessed from central memory circuit **550** and locally de-interleaved by a de-interleaver circuit **544**. De-interleaver circuit **544** re-arranges decoder output **548** to reverse the shuffling originally performed by interleaver circuit **542**. A resulting de-interleaved output **597** is provided to data detector circuit **530** where it is used to guide subsequent detection of a corresponding data set previously received as equalized output **525**.

Alternatively, where the decoded output converges (i.e., yields the originally written data set), the resulting decoded output is provided as an output codeword **572** to a de-interleaver circuit **580**. De-interleaver circuit **580** rearranges the data to reverse both the global and local interleaving applied to the data to yield a de-interleaved output **582**. De-interleaved output **582** is provided to a hard decision output circuit **590**. Hard decision output circuit **590** is operable to re-order data sets that may complete out of order back into their original order. The originally ordered data sets are then provided as a hard decision output **592**.

Data decoding circuit **570** provides an unsatisfied check value **528** to detector output combination circuit **523**. Unsatisfied check value **528** value indicates a number of errors remaining in decoder output **571** at the end of all local iterations through data decoder circuit **570** for a particular global iteration (i.e., at the end of the current global iteration). Detector output combination circuit **523** combines interleaved codeword **546** and previous interleaved codeword **527** based upon the number of remaining unsatisfied checks indicated by unsatisfied check value **528**. Of note, data processing system **500** is operable to process multiple data sets (i.e., sets of equalized data stored in input buffer **553**) concurrently. Thus, the number of unsatisfied checks that is used is specific to the currently processing data set.

Turning to FIG. **6**, an example implementation of a data detector output combination circuit **600** is depicted that may be used in relation to the embodiments of data processing system **500**. In some cases, data detector output combination circuit **600** may be used in place of output combination circuit **523**. In such cases, an unsatisfied checks input **628** is connected to unsatisfied check value **528**, a previous detector output **627** is connected to previous interleaved output **527**, a current detector output **646** is connected to interleaved output **546**, and a combined output **626** is connected to combined output **526**.

Data detector output combination circuit **600** includes an iteration weighting circuit **623** that provides a previous data scalar value (Wt1) **624** and a current data scalar value (Wt2) **688**. Previous detector output **627** is multiplied by previous data scalar value **624** by a multiplier circuit **636** to yield a previous product **687**; and current detector output **646** is multiplied by current data scalar value **688** by a multiplier circuit **630** to yield a current product **631**. A summation circuit adds current product **631** to previous product **687** to yield combined output **626**.

In one particular embodiment of the present invention, the values of Wt1 and Wt2 are as follows when the number of unsatisfied checks is greater than one hundred twenty eight (128):

Wt1=A; and

Wt2=B.

In one particular embodiment of the present invention, the value of A is zero (0), and the value of B is one (1). Where, on the other hand, the number of unsatisfied checks is less than or equal to one hundred twenty eight (128) and greater than thirty two (32), the values of Wt1 and Wt2 are as follows:

Wt1=C; and

Wt2=D.

In one particular embodiment of the present invention, the value of C is one (1), and the value of D is three (3). Alternatively, where the number of unsatisfied checks is less than or equal to thirty two (32), the values of Wt1 and Wt2 are as follows:

Wt1=E; and

Wt2=F.

In one particular embodiment of the present invention, the value of C is one (1), and the value of D is three (4). Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of different values for A, B, C, D, E, F, G and H that may be used in relation to different embodiments of the present invention. Such values may be either fixed or programmable. It should be noted that other threshold values (i.e., values other than 128 and 32) may be selected in accordance with different embodiments of the present invention. Such values may be either fixed or programmable.

Turning to FIG. **7**, another data processing system **700** including detector output reuse circuitry is shown in accordance with some embodiments of the present invention. Data processing system **700** includes an analog front end circuit **710** that receives an analog signal **705**. Analog front end circuit **710** processes analog signal **705** and provides a processed analog signal **712** to an analog to digital converter circuit **714**. Analog front end circuit **710** may include, but is not limited to, an analog filter and an amplifier circuit as are known in the art. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of circuitry that may be included as part of analog front end circuit **710**. In some cases, analog signal **705** is derived from a read/write head assembly (not shown) that is disposed in relation to a storage medium (not shown). In other cases, analog signal **705** is derived from a receiver circuit (not shown) that is operable to receive a signal from a transmission medium (not shown). The transmission medium may be wired or wireless. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of source from which analog input **705** may be derived.

Analog to digital converter circuit **714** converts processed analog signal **712** into a corresponding series of digital samples **716**. Analog to digital converter circuit **714** may be any circuit known in the art that is capable of producing digital samples corresponding to an analog input signal. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of analog to digital converter circuits that may be used in relation to different embodiments of the present invention. Digital samples **716** are provided to an equalizer circuit **720**. Equalizer circuit **720** applies an equalization algorithm to digital samples **716** to yield an equalized output **725**. In some embodiments of the present invention, equalizer circuit **720** is a digital finite impulse response filter circuit as are known in the art. It may be possible that equalized output **725** may be received

directly from a storage device in, for example, a solid state storage system. In such cases, analog front end circuit **710**, analog to digital converter circuit **714** and equalizer circuit **720** may be eliminated where the data is received as a digital data input. Equalized output **725** is stored to an input buffer **753** that includes sufficient memory to maintain one or more codewords until processing of that codeword is completed through a data detector circuit **730** and a data decoding circuit **770** including, where warranted, multiple global iterations (passes through both data detector circuit **730** and data decoding circuit **770**) and/or local iterations (passes through data decoding circuit **770** during a given global iteration). An output **757** is provided to data detector circuit **730**.

Data detector circuit **730** may be a single data detector circuit or may be two or more data detector circuits operating in parallel on different codewords. Whether it is a single data detector circuit or a number of data detector circuits operating in parallel, data detector circuit **730** is operable to apply a data detection algorithm to a received codeword or data set. In some embodiments of the present invention, data detector circuit **730** is a Viterbi algorithm data detector circuit as are known in the art. In other embodiments of the present invention, data detector circuit **730** is a is a maximum a posteriori data detector circuit as are known in the art. Of note, the general phrases "Viterbi data detection algorithm" or "Viterbi algorithm data detector circuit" are used in their broadest sense to mean any Viterbi detection algorithm or Viterbi algorithm detector circuit or variations thereof including, but not limited to, bi-direction Viterbi detection algorithm or bi-direction Viterbi algorithm detector circuit. Also, the general phrases "maximum a posteriori data detection algorithm" or "maximum a posteriori data detector circuit" are used in their broadest sense to mean any maximum a posteriori detection algorithm or detector circuit or variations thereof including, but not limited to, simplified maximum a posteriori data detection algorithm and a max-log maximum a posteriori data detection algorithm, or corresponding detector circuits. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of data detector circuits that may be used in relation to different embodiments of the present invention. In some cases, one data detector circuit included in data detector circuit **730** is used to apply the data detection algorithm to the received codeword for a first global iteration applied to the received codeword, and another data detector circuit included in data detector circuit **730** is operable apply the data detection algorithm to the received codeword guided by a decoded output accessed from a central memory circuit **750** on subsequent global iterations.

Upon completion of application of the data detection algorithm to the received codeword on the first global iteration, data detector circuit **730** provides a detector output **733**. Detector output **733** includes soft data. As used herein, the phrase "soft data" is used in its broadest sense to mean reliability data with each instance of the reliability data indicating a likelihood that a corresponding bit position or group of bit positions has been correctly detected. In some embodiments of the present invention, the soft data or reliability data is log likelihood ratio data as is known in the art. Detector output **733** is provided to a local interleaver circuit **742**. Local interleaver circuit **742** is operable to shuffle sub-portions (i.e., local chunks) of the data set included as detected output and provides an interleaved codeword **746**. Interleaver circuit **742** may be any circuit known in the art that is capable of shuffling data sets to yield a re-arranged data set.

Interleaved codeword **746** is provided to a detector output combination circuit **723** where it is combined with a previous interleaved codeword **727** accessed from central memory circuit **750** to yield a combined output **726**. Previous interleaved codeword **727** is derived from a detector output **733** resulting from a previous global iteration. Combined output **726** is stored to central memory circuit **750** as the current interleaved output, and the previous interleaved output is updated to be the current interleaved output in preparation for the next global iteration.

In a symbol based system, detector output combination circuit **723** determines a separation between the most likely symbol value and the second most likely symbol value. For example, where two bit symbols are used, four hard decision outputs are possible (0, 1, 2, 3), and interleaved codeword **746** provides four probability values corresponding to each of the respective outputs. In some embodiments of the present invention, the probability values are log likelihood ratio values. In such cases, detector output combination circuit **723** subtracts the second largest probability value from the largest probability value to yield a quality metric. A higher value quality metric corresponds to a higher quality detector output. Detector output combination circuit **723** combines interleaved codeword **746** and previous interleaved codeword **727** in a proportion based upon the quality.

Once a data decoding circuit **770** is available, the current interleaved output (i.e., the current instance of combined codeword **726**) is accessed from central memory circuit **750** as a stored codeword **786** and globally interleaved by a global interleaver/de-interleaver circuit **784**. Global interleaver/De-interleaver circuit **784** may be any circuit known in the art that is capable of globally rearranging codewords. Global interleaver/De-interleaver circuit **784** provides a decoder input **752** into data decoding circuit **770**. In some embodiments of the present invention, the data decode algorithm is a low density parity check algorithm as are known in the art. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize other decode algorithms that may be used in relation to different embodiments of the present invention. Data decoding circuit **770** applies a data decode algorithm to decoder input **752** to yield a decoded output **771**. In cases where another local iteration (i.e., another pass through data decoder circuit **770**) is desired, data decoding circuit **770** re-applies the data decode algorithm to decoder input **752** guided by decoded output **771**. This continues until either a maximum number of local iterations is exceeded or decoded output **771** converges.

Where decoded output **771** fails to converge (i.e., fails to yield the originally written data set) and a number of local iterations through data decoder circuit **770** exceeds maximum number of allowable local iterations, the resulting decoded output is provided as a decoded output **754** back to central memory circuit **750** where it is stored awaiting another global iteration through a data detector circuit included in data detector circuit **730**. Prior to storage of decoded output **754** to central memory circuit **750**, decoded output **754** is globally de-interleaved to yield a globally de-interleaved output **788** that is stored to central memory circuit **750**. The global de-interleaving reverses the global interleaving earlier applied to stored codeword **786** to yield decoder input **752**. When a data detector circuit included in data detector circuit **730** becomes available, a previously stored de-interleaved output **788** accessed from central memory circuit **750** and locally de-interleaved by a de-interleaver circuit **744**. De-interleaver circuit **744** re-arranges decoder output **748** to reverse the shuffling originally performed by interleaver circuit **742**. A resulting de-interleaved output **797** is provided to data detector circuit **730** where it is used to guide subsequent detection of a corresponding data set previously received as equalized output **725**.

Alternatively, where the decoded output converges (i.e., yields the originally written data set), the resulting decoded output is provided as an output codeword **772** to a de-interleaver circuit **780**. De-interleaver circuit **780** rearranges the data to reverse both the global and local interleaving applied to the data to yield a de-interleaved output **782**. De-interleaved output **782** is provided to a hard decision output circuit **790**. Hard decision output circuit **790** is operable to re-order data sets that may complete out of order back into their original order. The originally ordered data sets are then provided as a hard decision output **792**.

Turning to FIG. **8**, an example implementation of a data detector output combination circuit **800** is depicted that may be used in relation to the embodiments of data processing system **700**. In some cases, data detector output combination circuit **800** may be used in place of output combination circuit **723**. In such cases, a previous detector output **827** is connected to previous interleaved output **727**, a current detector output **846** is connected to interleaved output **746**, and a combined output **826** is connected to combined output **726**.

Data detector output combination circuit **800** includes a quality metric calculation circuit **893** that subtracts the second largest probability value for a given symbol of current detector output **846** from the largest probability value for the given symbol of current detector output **846** to yield a quality metric **822**. Quality metric **822** is provided to a quality based weighting circuit **883** that provides a previous data scalar value (Wt1) **824** based thereon. Previous detector output **827** is multiplied by previous data scalar value **824** by a multiplier circuit **836** to yield a previous product **887**. A summation circuit adds previous product **887** to current detector output **846** to yield combined output **826**.

In one particular embodiment of the present invention, the values of Wt1 is as follows: and Wt2 are as follows when the number of unsatisfied checks is greater than one hundred twenty eight (128):

$$Wt1 = \begin{cases} A, & \text{if } |\text{quality metric } 822| < \text{threshold } A \\ B, & \text{if threshold } A \le |\text{quality metric } 822| < \text{threshold } B \\ C, & \text{if threshold } B \le |\text{quality metric } 822| < \text{threshold } C \\ D, & \text{if } |\text{quality metric } 822| \ge \text{threshold } C \end{cases}$$

in one particular

The values of A, B, C, D, threshold A, threshold B, and threshold C may be wither fixed or programmable. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of different values for A, B, C, D, threshold A, threshold B, and threshold C that may be used in relation to different embodiments of the present invention.

It should be noted that the various blocks discussed in the above application may be implemented in integrated circuits along with other functionality. Such integrated circuits may include all of the functions of a given block, system or circuit, or a subset of the block, system or circuit. Further, elements of the blocks, systems or circuits may be implemented across multiple integrated circuits. Such integrated circuits may be any type of integrated circuit known in the art including, but are not limited to, a monolithic integrated circuit, a flip chip integrated circuit, a multichip module integrated circuit, and/or a mixed signal integrated circuit. It should also be noted that various functions of the blocks, systems or circuits discussed herein may be implemented in either software or firmware. In some such cases, the entire system, block or circuit may be implemented using its software or firmware equivalent. In other cases, the one part of a given system, block or circuit may be implemented in software or firmware, while other parts are implemented in hardware.

In conclusion, the invention provides novel systems, devices, methods and arrangements for data processing. While detailed descriptions of one or more embodiments of the invention have been given above, various alternatives, modifications, and equivalents will be apparent to those skilled in the art without varying from the spirit of the invention. Therefore, the above description should not be taken as limiting the scope of the invention, which is defined by the appended claims.

What is claimed is:

1. A data processing system, the data processing system comprising:

a data detector circuit operable to apply a data detection algorithm to a data input to yield a first detector output, and to reapply the data detection algorithm to the data input to yield a second detector output;

a combining circuit operable to combine a first input derived from the first detector output with a second input derived from the second detector output to yield a combined detector output, wherein the combined detector output includes a unified data set element generated by combining an element of the first input with a corresponding element of the second input;

a data decoder circuit operable to apply a data decoding algorithm to a decoder input derived from the combined detector output to yield a decoded output; and

wherein applying the data detection algorithm and applying the data decoding algorithm at least one time corresponds to a global iteration, and wherein the combining circuit is operable to combine the element of the first input with the corresponding element of the second input in a first proportion when the data decoding algorithm failed to converge and a number of global iterations is less than a threshold value and a second proportion when the data decoding algorithm failed to converge and the number of global iterations is greater than the threshold value, and wherein the first proportion is different from the second proportion.

2. The data processing system of claim **1**, wherein the decoder input is a first instance of the decoder input, and wherein reapplying the data detection algorithm to the data input to yield the second detector output is guided by a second instance of the decoder input.

3. The data processing system of claim **1**, wherein the system is implemented as an integrated circuit.

4. The data processing system of claim **1**, wherein the system is implemented as part of a device selected from a group consisting of: a communication device, and a storage device.

5. The data processing system of claim **1**, wherein the data decoder circuit is a low density parity check decoder circuit.

6. The data processing system of claim **1**, wherein the data detection algorithm is selected from a group consisting of: a Viterbi data detection algorithm, and a maximum a posterior data detection algorithm.

7. The data processing system of claim **1**, wherein the combined detector output is a first combined detector output, wherein the threshold value is a first threshold value, wherein the data detector circuit is further operable to apply the data detection algorithm to the data input to yield a third detector output, wherein the third detector output occurs coincident to the first threshold value, and wherein the combining circuit is further operable to combine the second input with a third input derived from the third detector output to yield a second

combined detector output when the number of global iterations is equal to a second threshold value.

8. A method for data processing, the method comprising:

applying a data detection algorithm using a data detector circuit to a data input to yield a first detector output;

re-applying the data detection algorithm using the data detector circuit to the data input to yield a second detector output;

combining a first input derived from the first detector output with a second input derived from the second detector output in a determined proportion to yield a combined detector output, wherein the determined proportion is selected from a group consisting of:

a first proportion when a data decoding algorithm failed to converge and a number of global iterations is less than a threshold value or a second proportion when the data decoding algorithm failed to converge and the number of global iterations is greater than the threshold value; and

a first proportion when a number of unsatisfied checks remaining in a decoded output is non-zero and exceeds a threshold value, and a second proportion when the number of unsatisfied checks is non-zero and is less than the threshold value; and

applying the data decoding algorithm using a data decoder circuit to a decoder input derived from the combined detector output to yield a decoded output and the number of unsatisfied checks remaining in the decoded output, wherein applying the data detection algorithm and applying the data decoding algorithm at least one time corresponds to the global iteration.

9. The method of claim **8**, wherein the combined detector output is a first combined detector output, wherein the threshold value is a first threshold value, and wherein the method further comprises:

re-applying the data detection algorithm to the data input to yield a third detector output, wherein the third detector output occurs coincident to the first threshold value; and

combining the second input with a third input derived from the third detector output to yield a second combined detector output when the number of global iterations is equal to a second threshold value.

10. The method of claim **8**, wherein the decoder input is a first instance of the decoder input, and wherein reapplying the data detection algorithm to the data input to yield the second detector output is guided by a second instance of the decoder input.

11. The method of claim **8**, wherein the data decoder circuit is a low density parity check decoder circuit, and wherein the data detection algorithm is selected from a group consisting of: a Viterbi data detection algorithm, and a maximum a posterior data detection algorithm.

12. A data processing system, the data processing system comprising:

a data detector circuit operable to apply a data detection algorithm to a data input to yield a first detector output, and to reapply the data detection algorithm to the data input to yield a second detector output;

a combining circuit operable to combine a first input derived from the first detector output with a second input derived from the second detector output to yield a combined detector output;

a data decoder circuit operable to apply a data decoding algorithm to a decoder input derived from the combined detector output to yield a decoded output and a number of unsatisfied checks; and

wherein the combining circuit is operable to combine the first input with the second input in a first proportion when the number of unsatisfied checks is non-zero and exceeds a threshold value, and a second proportion when the number of unsatisfied checks is non-zero and is less than the threshold value.

13. The data processing system of claim **12**, wherein the system is implemented as an integrated circuit.

14. The data processing system of claim **12**, wherein the system is implemented as part of a device selected from a group consisting of: a communication device, and a storage device.

15. The data processing system of claim **12**, wherein the system is implemented as an integrated circuit.

16. A data processing system, the data processing system comprising:

a data detector circuit operable to apply a data detection algorithm to a data input to yield a first detector output, and to reapply the data detection algorithm to the data input to yield a second detector output;

a combining circuit operable to combine a first input derived from the first detector output with a second input derived from the second detector output to yield a combined detector output;

a data decoder circuit operable to apply a data decoding algorithm to a decoder input derived from the combined detector output to yield a decoded output and a number of unsatisfied checks; and

wherein the combining circuit is further operable to generate a quality metric indicative of a quality of an element of the first input, and wherein the combining circuit is operable to combine the first input with the second input in a first proportion when a number of unsatisfied checks after application of the data decoding algorithm is non-zero and the quality metric exceeds a threshold value, and a second proportion when the number of unsatisfied checks is non-zero and the quality metric is less than the threshold value.

17. The data processing system of claim **16**, wherein the system is implemented as an integrated circuit.

18. The data processing system of claim **16**, wherein the system is implemented as part of a device selected from a group consisting of: a communication device, and a storage device.

19. The data processing system of claim **16**, wherein the system is implemented as an integrated circuit.

20. The data processing system of claim **16**, wherein the decoder input is a first instance of the decoder input, and wherein reapplying the data detection algorithm to the data input to yield the second detector output is guided by a second instance of the decoder input.

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